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SH-2A, SH-2 E200F Emulator

Additional Document for User's Manual

Supplementary Information on Using the SH2A_custom_SoC

Renesas Microcomputer Development Environment System

SuperH™ Family / SH7200 Series

E200F for SH2A_custom_SoC R0E507200EMU00E

User's Manual

Rev.2.00
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Section 1 System Configuration

1.1 Components of the Emulator

The E200F emulator supports the SH2A_custom_SoC_1 and SH2A_custom_SoC_2. For the selection of the SH2A_custom_SoC_1 or SH2A_custom_SoC_2 when using the emulator, ask Renesas Technology Corp. via the sales office.

Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

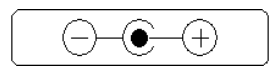
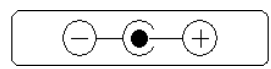
Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Emulator main unit		1	R0E0200F1EMU00: Depth: 195.0 mm, Width: 130.0 mm, Height: 45.0 mm, Mass: 490.0 g
	AC adapter	Product numbers: 0001 to 0113		
			1	Input: 100 to 240 V Output: 12 V 4.0 A Depth: 120.0 mm, Width: 72.0 mm, Height: 27.0 mm, Mass: 400.0 g 
		Product numbers: 0114 or later		
			1	Input: 100 to 240 V Output: 12 V 3.0 A Depth: 99.0 mm, Width: 62.0 mm, Height: 26.0 mm, Mass: 270.0 g 
	AC cable		1	Length: 2000 mm

Table 1.1 Components of the Emulator (cont)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware (cont)	USB cable		1	Length: 1500 mm, Mass: 50.6 g
	External probe	Product numbers: 0001 to 0113		
			1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
		Product numbers: 0114 or after		
			1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
Soft-ware	E200F emulator setup program, SH-2A, SH-2 E200F Emulator User's Manual, and Supplementary Information on Using the SH2A_custom_SoC*		1	R0E0200F1EMU00S, R0E0200F1EMU00J, R0E0200F1EMU00E, R0E507200EMU00J, and R0E507200EMU00E (provided on a CD-R)

Note: Additional document for the MCUs supported by the emulator is included. Check the target MCU and refer to its additional document.

Table 1.2 Optional Components of the Emulator

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	External bus trace unit		1	R0E0200F1ETU00: Depth: 90.0 mm, Width: 125.0 mm, Height: 15.2 mm, Mass: 83 g
	Emulation memory unit (Memory capacity: 8 Mbytes or 16 Mbytes)		1	R0E0200F1MSR00 (8 Mbytes), R0E0200F1MSR01 (16 Mbytes): Depth: 90.0 mm, Width: 125.0 mm, Height: 15.2 mm, Mass: 81 g (R0E0200F1MSR00), 85 g (R0E0200F1MSR01) Note that it is not possible to connect these emulation memory units at the same time.
	Trace cable		1	R0E0200F0ACC00: Length: 300 mm, Mass: 65 g
	Expansion profiling unit		1	R0E0200F0EPU00: Depth: 98.0 mm, Width: 115.0 mm, Height: 15.2 mm, Mass: 52 g

1.2 System Configuration

Figure 1.1 shows an example of the emulator system configuration.

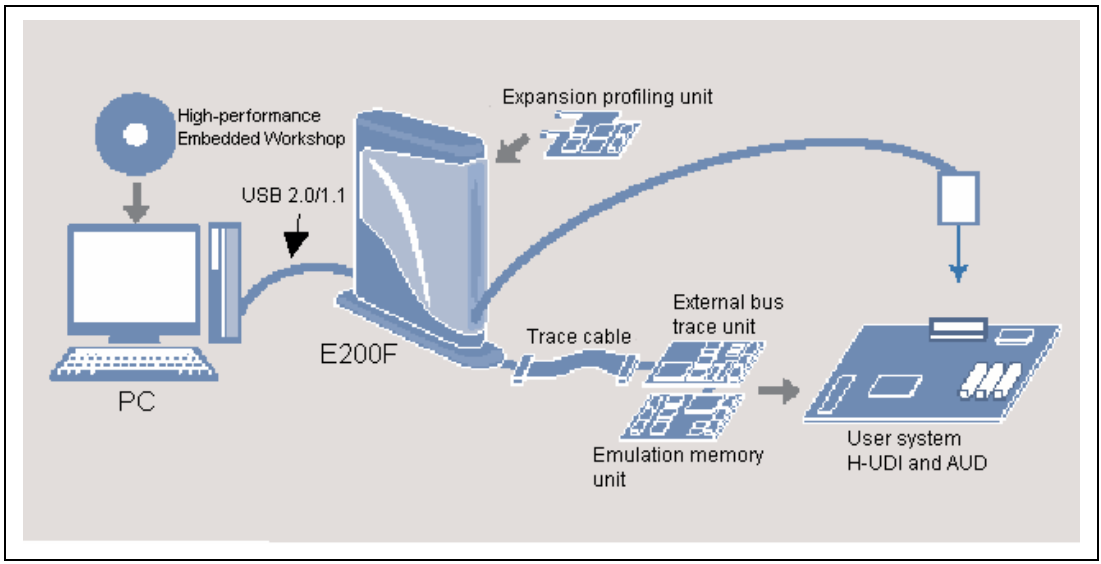


Figure 1.1 System Configuration Using the Emulator

(1) System Configuration of the SH2A_custom_SoC

Table 1.3 shows the system configuration supported by the SH2A_custom_SoC.

Table 1.3 System Configuration Supported by the SH2A_custom_SoC E200F

	E200F Emulator	External Bus Trace Unit	Emulation Memory Unit	Expansion Profiling Unit	Trace Cable
	R0E0200F1EMU00	R0E0200F1ETU00	R0E0200F1MSR00 R0E0200F1MSR01	R0E0200F0EPU00	R0E0200F0ACC00
System configuration 1	Supported	Not supported	Not supported	Not supported	Not supported
System configuration 2	Supported	Supported	Not supported	Not supported	Supported
System configuration 3	Supported	Supported	Supported	Not supported	Supported
System configuration 4	Supported	Not supported	Supported	Not supported	Supported
System configuration 5	Supported	Not supported	Not supported	Not supported	Supported
System configuration 6	Supported	Not supported	Not supported	Supported	Not supported
System configuration 7	Supported	Supported	Not supported	Supported	Supported
System configuration 8	Supported	Supported	Supported	Supported	Supported
System configuration 9	Supported	Not supported	Supported	Supported	Supported
System configuration 10	Supported	Not supported	Not supported	Supported	Supported

Section 2 Connecting the Emulator to the User System

2.1 Connecting the Emulator to the User System

When the emulator is connected to the user system, use the optional external bus trace unit and trace cable.

2.2 Connecting the Emulator to the User System by Using the H-UDI Port Connector

To connect the E200F emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MCU.

It is impossible to connect the emulator to the 14-pin type connector that is recommended for the E10A-USB emulator. The 36-pin type connector is the same as that of the E10A-USB emulator. When designing the user system, read the E200F emulator user's manual and hardware manual for the related device.

Table 2.1 shows the type number of the emulator, the corresponding connector type, and the use of AUD function.

Table 2.1 Type Number, AUD Function, and Connector Type

Type Number	Connector	AUD Function
R0E200F1EMU00	14-pin connector	Not available
R0E200F1EMU00	36-pin connector	Available

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use the 36-pin connector when using the emulator.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. This connector type is not available for the emulator. Use the E10A-USB emulator.

2.3 Installing the H-UDI Port Connector on the User System

Table 2.2 shows the recommended H-UDI port connectors for the emulator.

Table 2.2 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type

Note: When designing the 36-pin connector layout on the user board, do not connect any components under the H-UDI connector.

2.4 Pin Assignments of the H-UDI Port Connector

Figure 2.1 shows the pin assignments of the 36-pin H-UDI port connectors.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following page differ from those of the connector manufacturer.

Pin No.	Signal	Input/ Output*1	Note	Pin No.	Signal	Input/ Output*1	Note
1	AUDCK	Output		19	TMS	Input	
2	GND	——		20	GND	——	
3	AUDATA0	Output		21	_TRST*2	Input	
4	GND	——		22	(GND)*4	——	
5	AUDATA1	Output		23	TDI	Input	
6	GND	——		24	GND	——	
7	AUDATA2	Output		25	TDO	Output	
8	GND	——		26	GND	——	
9	AUDATA3	Output		27	_ASEBRKAK /_ASEBRK*2	Input/ output	
10	GND	——		28	GND	——	
11	_AUDSYNC*2	Output		29	UVCC	Output	
12	GND	——		30	GND	——	
13	N.C.	——		31	_RES*2	Output	User reset
14	GND	——		32	GND	——	
15	N.C.	——		33	GND*3	Output	
16	GND	——		34	GND	——	
17	TCK	Input		35	N.C.	——	
18	GND	——		36	GND	——	

Notes: 1. Input to or output from the user system.
2. The symbol (_) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. When the E200F probe head is connected to this pin and the _ASEMD pin is set to 0, do not connect to GND but to the _ASEMD pin directly.

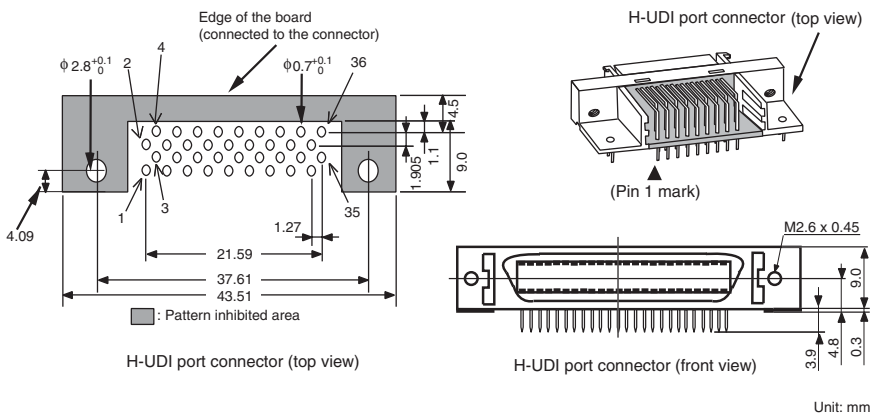


Figure 2.1 Pin Assignments of the H-UDI Port Connector (36 Pins)

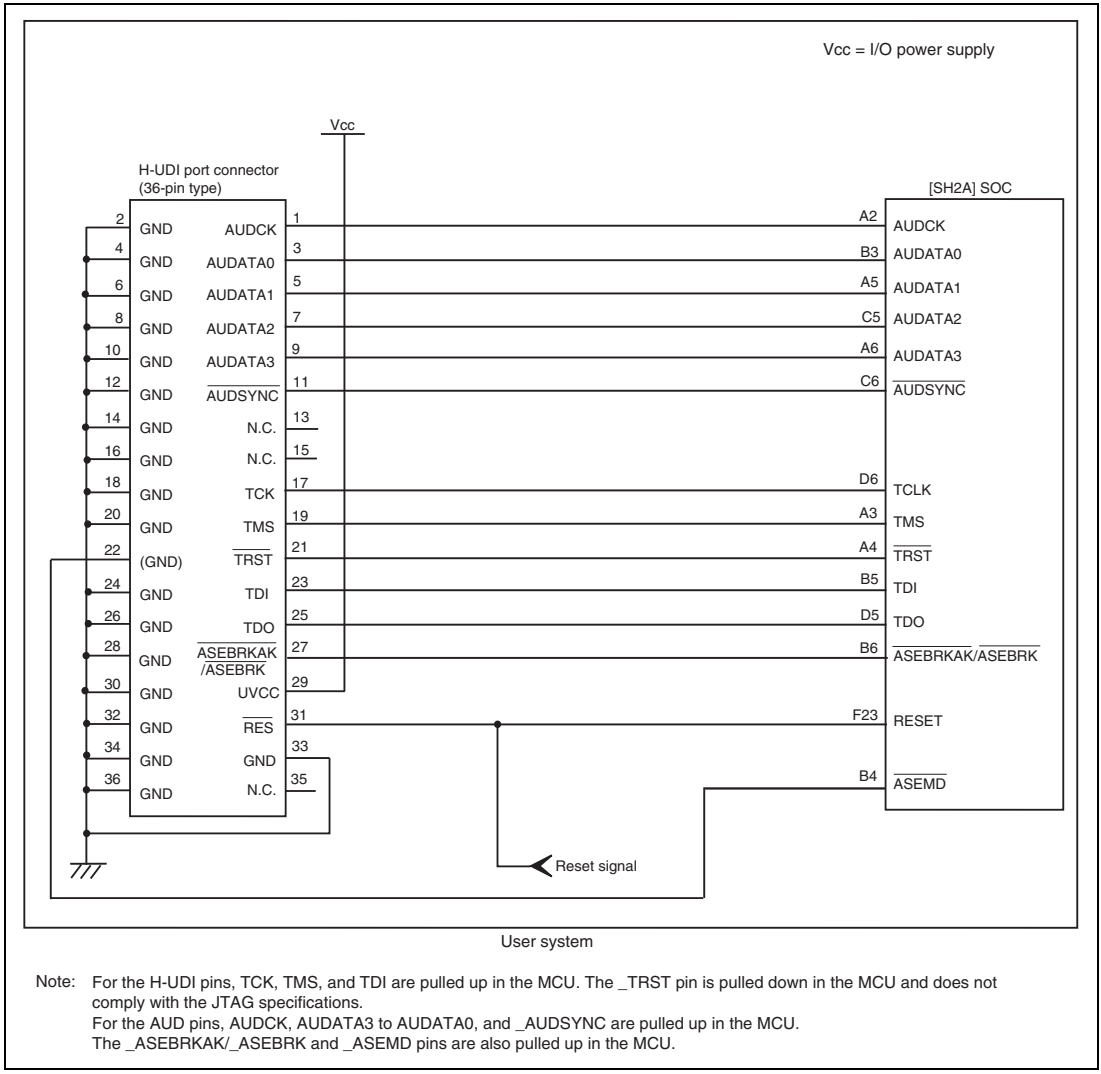
2.5 Recommended Circuit between the H-UDI Port Connector and the MCU

2.5.1 Recommended Circuit (36-Pin Type)

Figure 2.2 shows a recommended circuit for connection between the H-UDI and AUD port connectors (36 pins) and the MCU when the emulator is in use.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.

2. The _ASEMD pin must be 0 when the emulator is connected and 1 when the emulator is not connected, respectively.
   (1) When the emulator is used: _ASEMD = 0 (ASE mode)
   (2) When the emulator is not used: _ASEMD = 1 (normal mode)
   Figure 2.2 shows an example of circuits that allow the _ASEMD pin to be GND (0) whenever the emulator is connected by using the user system interface cable.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The pattern between the H-UDI port connector and the MCU must be as short as possible. Do not connect the signal lines to other components on the board.
5. The AUD signals (AUDCK, AUDATA3 to AUDATA0, and _AUDSYNC) operate in high speed. Isometric connection is needed if possible. Do not separate connection nor connect other signal lines adjacently.
6. Since the H-UDI and the AUD of the MCU operate with the PVcc, supply only the PVcc to the UVCC pin.
7. The resistance values shown in figure 2.2 are for reference.
8. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MCU.



Note: For the H-UDI pins, TCK, TMS, and TDI are pulled up in the MCU. The _TRST pin is pulled down in the MCU and does not comply with the JTAG specifications.
For the AUD pins, AUDCK, AUDATA3 to AUDATA0, and _AUDSYNC are pulled up in the MCU.
The _ASEBRKAK/_ASEBRK and _ASEMD pins are also pulled up in the MCU.

Figure 2.2 Recommended Circuit for Connection between the H-UDI Port Connector and MCU when the Emulator is in Use (36-Pin Type)

2.6 Connecting the E200F External Bus Trace Unit with the User System

To use the external bus trace function in the emulator, the emulator and the user system must be connected via the external bus trace unit (R0E0200F1ETU00). Install the connector on the user system for connection of the external bus trace unit, referring to section 2.7, Installing the External Bus Trace Unit Connector, in this manual. When designing the user system, read the SH-2A, SH-2 E200F Emulator User's Manual and hardware manual for the related MCU.

2.7 Installing the External Bus Trace Unit Connector

2.7.1 External Bus Trace Unit Connector Installed on the User System

Table 2.3 shows the recommended external bus trace unit connector.

Table 2.3 Recommended Connector

Type Number	Manufacturer	Specification
QTH-090-04-L-D-A	Samtec, Inc.	QTH series, 0.5-mm pitch, 180 pins

Note: Do not place any components within 6 mm of the external bus trace unit connector.

2.7.2 Pin Assignments of the User System Connector

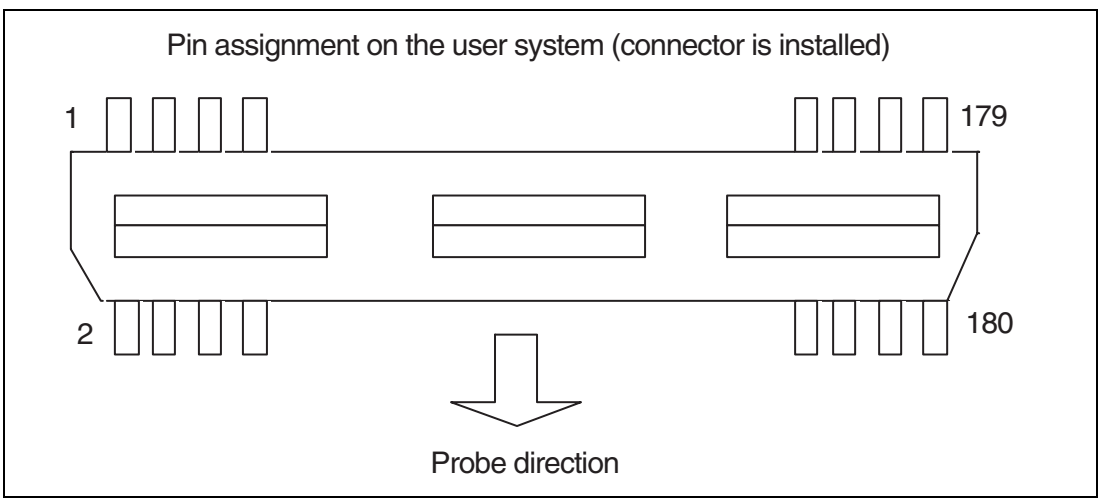


Figure 2.3 Pin Assignments of the User System Connector

2.7.3 Recommended Pad Pattern

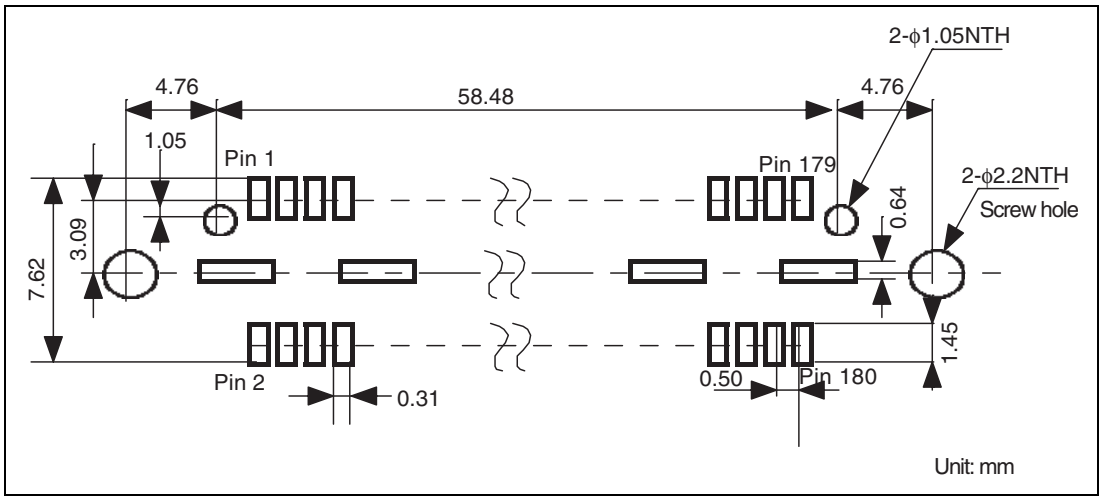


Figure 2.4 Recommended Pad Pattern (on which the Connector is Installed)

2.7.4 Restrictions on Component Installation

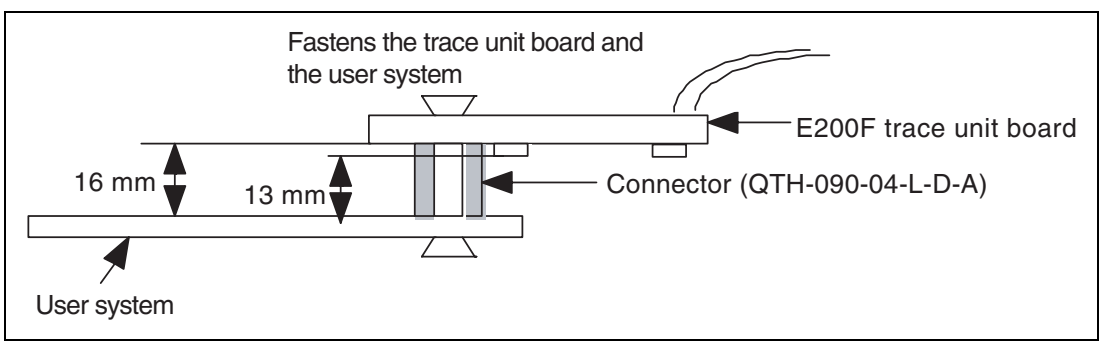


Figure 2.5 Restrictions on Component Installation

2.7.5 Pin Assignments of the External Bus Trace Unit Connector

Table 2.4 shows the pin assignments of the external bus trace unit connector.

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
1	I	UA-P0	-	3.3 V	Address bus	Fix this pin to low level.
2	I	UA-P1	CA1	3.3 V	Address bus	Connect the address signal of the MPU.
3	I	UA-P2	CA2	3.3 V	Address bus	Same as above.
4	I	UA-P3	CA3	3.3 V	Address bus	Same as above.
5	I	UA-P4	CA4	3.3 V	Address bus	Same as above.
6	I	UA-P5	CA5	3.3 V	Address bus	Same as above.
7	I	UA-P6	CA6	3.3 V	Address bus	Same as above.
8	I	UA-P7	CA7	3.3 V	Address bus	Same as above.
9	-	GND	GND		GND	GND
10	-	GND	GND		GND	GND
11	I	UA-P8	CA8	3.3 V	Address bus	Connect the address signal of the MPU.
12	I	UA-P9	CA9	3.3 V	Address bus	Same as above.
13	I	UA-P10	CA10	3.3 V	Address bus	Same as above.
14	I	UA-P11	CA11	3.3 V	Address bus	Same as above.
15	I	UA-P12	CA12	3.3 V	Address bus	Same as above.
16	I	UA-P13	CA13	3.3 V	Address bus	Same as above.
17	I	UA-P14	CA14	3.3 V	Address bus	Same as above.
18	I	UA-P15	CA15	3.3 V	Address bus	Same as above.
19	-	GND	GND		GND	GND
20	-	GND	GND		GND	GND
21	I	UA-P16	CA16	3.3 V	Address bus	Connect the address signal of the MPU.
22	I	UA-P17	CA17	3.3 V	Address bus	Same as above.
23	I	UA-P18	CA18	3.3 V	Address bus	Same as above.
24	I	UA-P19	CA19	3.3 V	Address bus	Same as above.
25	I	UA-P20	CA20	3.3 V	Address bus	Same as above.

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
26	I	UA-P21	CA21	3.3 V	Address bus	Same as above.
27	I	UA-P22	CA22	3.3 V	Address bus	Same as above.
28	I	UA-P23	CA23	3.3 V	Address bus	Same as above.
29	-	GND	GND		GND	GND
30	-	GND	GND		GND	GND
31	I	UA-P24	-	3.3 V	Reserved	Fix this pin to low level.
32	I	UA-P25	-	3.3 V	Reserved	Same as above.
33	I	UA-P26	-	3.3 V	Reserved	Same as above.
34	I	UA-P27	-	3.3 V	Reserved	Same as above.
35	I	UA-P28	-	3.3 V	Reserved	Same as above.
36	I	UA-P29	-	3.3 V	Reserved	Same as above.
37	I	UA-P30	-	3.3 V	Reserved	Same as above.
38	I	UA-P31	-	3.3 V	Reserved	Same as above.
39	-	GND	GND		GND	GND
40	-	GND	GND		GND	GND
41	IO	UD-P0	CD0	3.3 V	Data bus	Connect the data signal of the MPU.
42	IO	UD-P1	CD1	3.3 V	Data bus	Same as above.
43	IO	UD-P2	CD2	3.3 V	Data bus	Same as above.
44	IO	UD-P3	CD3	3.3 V	Data bus	Same as above.
45	IO	UD-P4	CD4	3.3 V	Data bus	Same as above.
46	IO	UD-P5	CD5	3.3 V	Data bus	Same as above.
47	IO	UD-P6	CD6	3.3 V	Data bus	Same as above.
48	IO	UD-P7	CD7	3.3 V	Data bus	Same as above.
49	-	GND	GND		GND	GND
50	-	GND	GND		GND	GND
51	IO	UD-P8	CD8	3.3 V	Data bus	Connect the data signal of the MPU.
52	IO	UD-P9	CD9	3.3 V	Data bus	Same as above.
53	IO	UD-P10	CD10	3.3 V	Data bus	Same as above.

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F						
Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
54	IO	UD-P11	CD11	3.3 V	Data bus	Same as above.
55	IO	UD-P12	CD12	3.3 V	Data bus	Same as above.
56	IO	UD-P13	CD13	3.3 V	Data bus	Same as above.
57	IO	UD-P14	CD14	3.3 V	Data bus	Same as above.
58	IO	UD-P15	CD15	3.3 V	Data bus	Same as above.
59	-	GND	GND		GND	GND
60	-	GND	GND		GND	GND
61	IO	UD-P16	N.C.	3.3 V	Data bus	N.C.
62	IO	UD-P17	N.C.	3.3 V	Data bus	N.C.
63	IO	UD-P18	N.C.	3.3 V	Data bus	N.C.
64	IO	UD-P19	N.C.	3.3 V	Data bus	N.C.
65	IO	UD-P20	N.C.	3.3 V	Data bus	N.C.
66	IO	UD-P21	N.C.	3.3 V	Data bus	N.C.
67	IO	UD-P22	N.C.	3.3 V	Data bus	N.C.
68	IO	UD-P23	N.C.	3.3 V	Data bus	N.C.
69	-	GND	GND		GND	GND
70	-	GND	GND		GND	GND
71	IO	UD-P24	N.C.	3.3 V	Data bus	N.C.
72	IO	UD-P25	N.C.	3.3 V	Data bus	N.C.
73	IO	UD-P26	N.C.	3.3 V	Data bus	N.C.
74	IO	UD-P27	N.C.	3.3 V	Data bus	N.C.
75	IO	UD-P28	N.C.	3.3 V	Data bus	N.C.
76	IO	UD-P29	N.C.	3.3 V	Data bus	N.C.
77	IO	UD-P30	N.C.	3.3 V	Data bus	N.C.
78	IO	UD-P31	N.C.	3.3 V	Data bus	N.C.
79	-	GND	GND		GND	GND
80	-	GND	GND		GND	GND

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
81	IO	UD-P32	xSRAS	3.3 V	SDRAM	_RASL (Fix _RASL to high level when it is not used.)
82	IO	UD-P33	-	3.3 V	Reserved	Fix this pin to high level.
83	IO	UD-P34	xSCAS	3.3 V	SDRAM	_CASL (Fix _CASL to high level when it is not used.)
84	IO	UD-P35	-	3.3 V	Reserved	Fix this pin to high level.
85	IO	UD-P36	CDQML		SDRAM	CDQML
86	IO	UD-P37	CDQMU		SDRAM	CDQMU
87	IO	UD-P38	-		Reserved (SDRAM)	Fix this pin to high level.
88	IO	UD-P39	-	3.3 V	Reserved (SDRAM)	Fix this pin to high level.
89	-	GND	GND		GND	GND
90	-	GND	GND		GND	GND
91	IO	UD-P40	-	3.3 V	Read/write signal	Fix this pin to high level.
92	IO	UD-P41	N.C.		Reserved	N.C.
93	IO	UD-P42	N.C.		Reserved	N.C.
94	IO	UD-P43	N.C.		Reserved	N.C.
95	IO	UD-P44	N.C.		Reserved	N.C.
96	IO	UD-P45	N.C.		Reserved	N.C.
97	IO	UD-P46	N.C.		Reserved	N.C.
98	IO	UD-P47	N.C.		Reserved	N.C.
99	-	GND	GND		GND	GND
100	-	GND	GND		GND	GND
101	IO	UD-P48	-	3.3 V	Reserved	Fix this pin to high level.
102	IO	UD-P49	-	3.3 V	Reserved	Same as above.
103	IO	UD-P50	-	3.3 V	Reserved	Same as above.
104	IO	UD-P51	-	3.3 V	Reserved	Same as above.
105	IO	UD-P52	-	3.3 V	Reserved	Same as above.

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
106	IO	UD-P53	-	3.3 V	Reserved	Same as above.
107	IO	UD-P54	-	3.3 V	Reserved	Same as above.
108	IO	UD-P55	-	3.3 V	Reserved	Same as above.
109	-	GND	GND		GND	GND
110	-	GND	GND		GND	GND
111	IO	UD-P56	-		Reserved	Fix this pin to high level.
112	IO	UD-P57	-		Reserved	Same as above.
113	IO	UD-P58	-		Reserved	Same as above.
114	IO	UD-P59	-		Reserved	Same as above.
115	IO	UD-P60	-		Reserved	Same as above.
116	IO	UD-P61	-		Reserved	Same as above.
117	IO	UD-P62	-		Reserved	Same as above.
118	IO	UD-P63	-		Reserved	Same as above.
119	-	GND	GND		GND	GND
120	-	GND	GND		GND	GND
121	I	UCONT-P0	xIWE0	3.3 V	Write strobe/SDRAM	_WE0: necessary
122	I	UCONT-P1	xIWE1	3.3 V	Write strobe/SDRAM	_WE1: necessary
123	I	UCONT-P2	-	3.3 V	Reserved	Fix this pin to high level.
124	I	UCONT-P3	-	3.3 V	Reserved	Same as above.
125	I	UCONT-P4	XIRD	3.3 V	Read strobe	_RD: necessary
126	I	UCONT-P5	XBS	3.3 V	Bus cycle start signal	_BS (Fix _BS to high level when it is not used.)
127	I	UCONT-P6	N.C.		Reserved	N.C.
128	I	UCONT-P7	N.C.		-	N.C.
129	I	UCONT-P8	N.C.		-	N.C.
130	I	UCONT-P9	N.C.		-	N.C.

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
131	I	UCONT-P10	N.C.		Reserved	N.C.
132	I	UCONT-P11	N.C.		Reserved	N.C.
133	I	UCONT-P12	N.C.		Reserved	N.C.
134	I	UCONT-P13	N.C.		Reserved	N.C.
135	I	UCONT-P14	N.C.		-	N.C.
136	I	UCONT-P15	N.C.		-	N.C.
137	I	UCONT-P16	-	3.3 V	Reserved	Fix this pin to high level.
138	I	UCONT-P17	-	3.3 V	Reserved	Same as above.
139	I	UCONT-P18	-	3.3 V	Reserved	Same as above.
140	I	UCONT-P19	-	3.3 V	Reserved	Same as above.
141	I	UCONT-P20	xRESET	3.3 V	Power-on reset request	_RES: necessary
142	I	UCONT-P21	xWAITI	3.3 V	Hardware wait request	_WAIT (Fix _WAIT to high level when it is not used.)
143	I	UCONT-P22	-	3.3 V	Reserved	Fix this pin to high level.
144	I	UCONT-P23	NMI	3.3 V	Non-maskable interrupt request	NMI (Fix NMI to high level when it is not used.)
145	I	UCONT-P24	N.C.		-	N.C.
146	I	UCONT-P25	N.C.		-	N.C.
147	I	UCONT-P26	N.C.		-	N.C.
148	I	UCONT-P27	N.C.		-	N.C.
149	I	UCONT-P28	N.C.		-	N.C.
150	I	UCONT-P29	N.C.		-	N.C.
151	I	UCONT-P30	N.C.		-	N.C.
152	I	UCONT-P31	N.C.		-	N.C.
153	-	GND	GND		GND	GND
154	-	GND	GND		GND	GND
155	I	MPUCLK	BCLK	3.3 V	Bus clock	BCLK: necessary

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
156	-	GND	GND		GND	GND
157	-	GND	GND		GND	GND
158	I	DDRCLK	GND		GND	GND
159	-	GND	GND		GND	GND
160	I	DDRCLK-N	GND		GND	GND
161	-	GND	GND		GND	GND
162	-	GND	GND		GND	GND
163	I	CS0IN-N	xCS0	3.3 V	Chip select signal	Connect _CS* (chip select). Fix the unused _CS* pin to high level.
164	I	CS1IN-N	-	3.3 V	Reserved	Fix this pin to high level.
165	I	CS2IN-N	xCS2	3.3 V	Reserved	Same as above.
166	I	CS3IN-N	xCS3	3.3 V	Chip select signal	Connect _CS* (chip select). Fix the unused _CS* pin to high level.
167	I	CS4IN-N	-	3.3 V	Reserved	Fix this pin to high level.
168	I	CS5IN-N	-	3.3 V	Chip select signal	Connect _CS* (chip select). Fix the unused _CS* pin to high level.
169	I	CS6IN-N	-	3.3 V	Reserved	Fix this pin to high level.
170	I	CS7IN-N	-	3.3 V	Reserved	Same as above.
171	I	CS8IN-N	-	3.3 V	Reserved	Same as above.
172	I	CS9IN-N	N.C.		-	N.C.
173	O	EM0OUT-N	N.C.		-	N.C.
174	O	EM1OUT-N	N.C.		-	N.C.
175	O	EM2OUT-N	N.C.		-	N.C.
176	O	EMEN-P	N.C.		-	N.C.
177	I	VCCQ	VCC	3.3 V	Power supply for user system: 3.3 V	Connect VCCQ.
178	I	VCCQ	VCC	3.3 V	Power supply for user system: 3.3 V	Connect VCCQ.

Table 2.4 Pin Assignments of the External Bus Trace Unit Connector (cont)

E200F External Trace Bus I/F

Pin No.	I/O (CONT)	E200F Trace I/F Connector Pin Name	SH2A_ custom_ SoC Signal Name	Voltage	Meaning of Signal	Note
179	I	VCCQ	VCC	3.3 V	Power supply for user system: 3.3 V	Connect VCCQ.
180	I	GND	GND		GND	Input low level or connect GND.

Note: Voltage-applying level: H: 2.4V to VCCQ, L: GND to 0.4V.
N.C.: Do not connect anything to this pin. Fix the unused signals of the address or data bus to high or low level.
For multiplexed pins, connect a pin such that the signal name and the signal used by the user are matched.
Be sure to connect the signals written as 'necessary', GND, and VCCQ to operate the emulator normally.
If a signal input pin such as an address pin is fixed to high or low (GND) level, the actual CPU access may differ in trace display or condition access.

2.7.6 Layout of the External Bus Trace Unit Connector

When designing the user system, there are restrictions on the position to install the external bus trace unit connector. Figure 2.6 shows the external dimensions of the external bus trace unit.

The size of the printed-circuit board of the E200F external bus trace unit is 90 mm × 125 mm. The size of components around the user system connector must not exceed the limit on component installation (the height must be 10 mm or less).

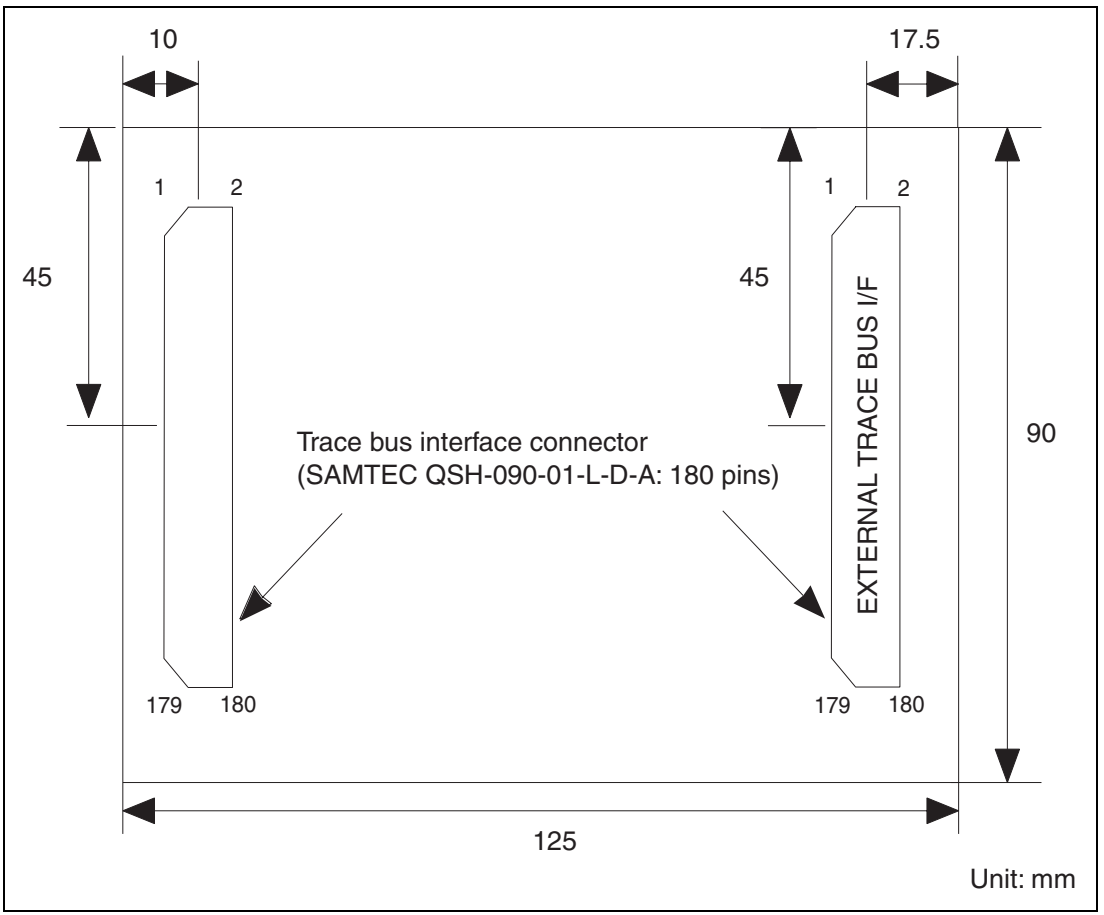


Figure 2.6 External Dimensions of the External Bus Trace Unit (on which the Connector is Installed)

Notes: 1. The external bus trace interface connector installed on the user system must be as close to the MPU as possible.

2. Wiring pattern of clock lines
   The followings are notes on wiring of clock lines for the E200F trace interface signals. Take them into consideration when designing the user system to embed suitable clock lines.
   (a) Clock lines must be as short as possible.
   (b) Clock lines must be surrounded by the GND pattern for protection so that the signals will be of low-impedance.
   (c) Other layers next to the layer with clock line wiring should have solid patterns of GND/VCC so that the signals will be of low-impedance.
   (d) To prevent affect by the crosstalk noise, other signal patterns must not be embedded along with the clock lines.

2.8 Connecting the External Bus Trace Unit to the User System

This section describes how to connect the external bus trace unit and emulation memory unit to the user system.

2.8.1 Connecting the E200F External Bus Trace Unit to the Emulator Main Unit

- Open the cover of TRACE I/F on the side of the main unit case.
- Connect the trace cable provided for the external bus trace unit to the emulator as shown in figure 2.7.

Figure 2.7 Connecting the Trace Cable to E200F

- Connect the external bus trace unit to the trace cable (CN1 side).

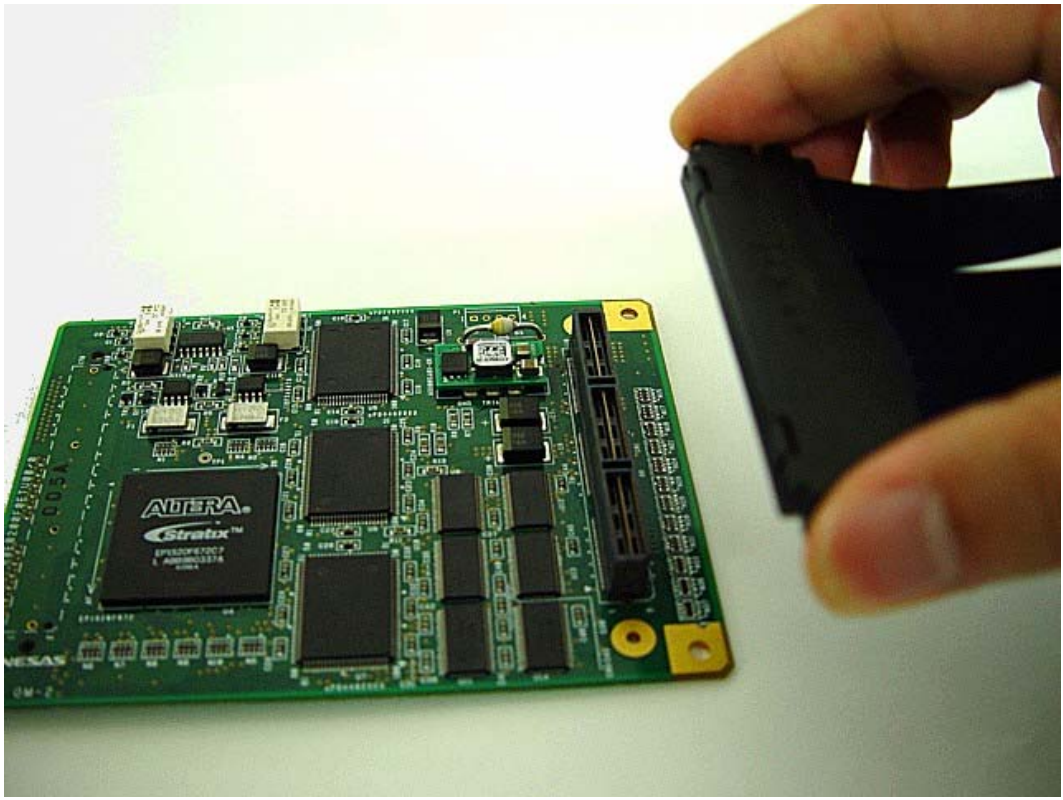


Figure 2.8 Connecting the Trace Cable to the External Bus Trace Unit

2.8.2 Connecting the E200F External Bus Trace Unit to the User System

- After checking the location of pin 1, connect the user system to the external bus trace unit.

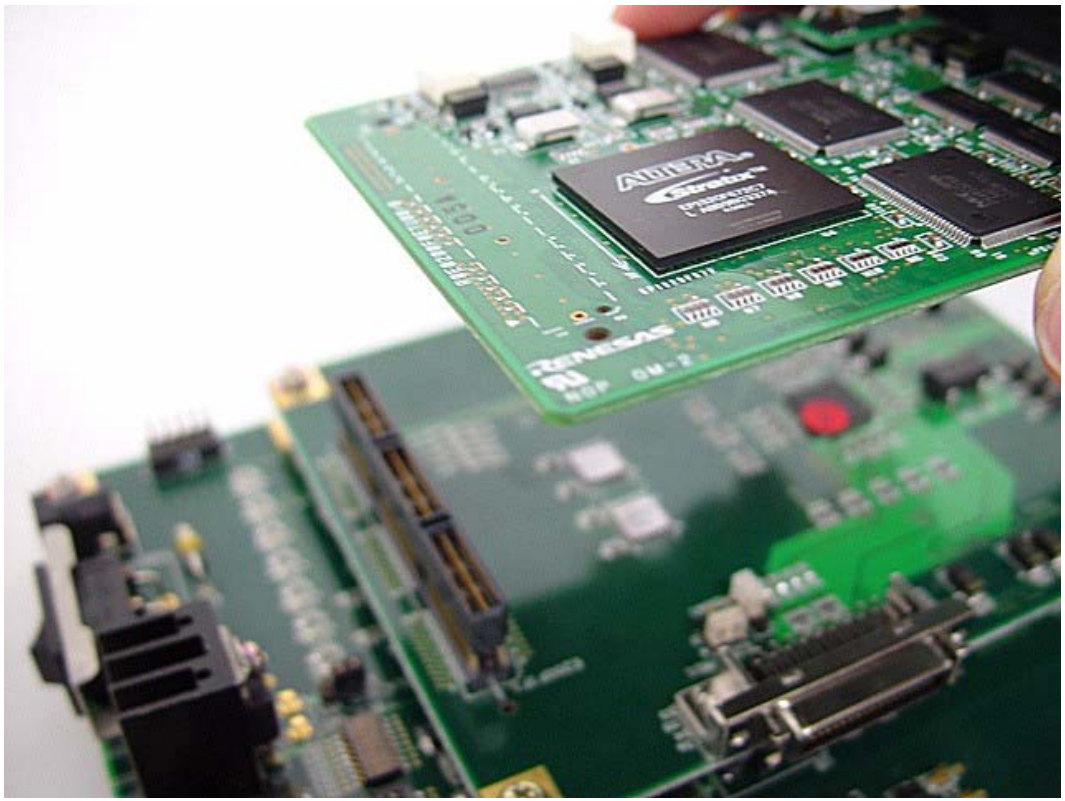


Figure 2.9 Connecting the User System to the External Bus Trace Unit

⚠ CAUTION
Check the location of pin 1 before connecting.

Note: Connection of the signals differs depending on the MCU used.

2.8.3 Connecting the E200F Emulation Memory Unit to the Emulator Main Unit

- Open the cover of TRACE I/F on the side of the main unit case.
- Connect the trace cable provided for the external bus trace unit to the emulator as shown in figure 2.10.

Figure 2.10 Connecting the Trace Cable to E200F

- Connect the emulation memory unit to the trace cable (CN1 side).

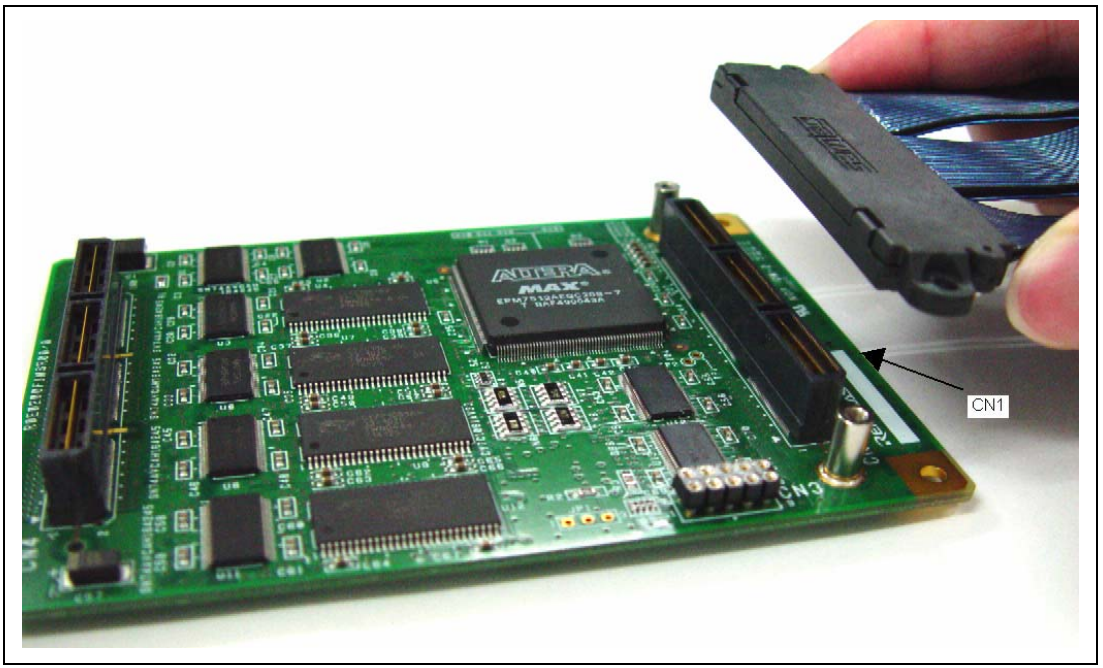


Figure 2.11 Connecting the Trace Cable to the Emulation Memory Unit

2.8.4 Connecting the Emulation Memory Unit to the User System

- After checking the location of pin 1, connect the user system to the emulation memory unit.

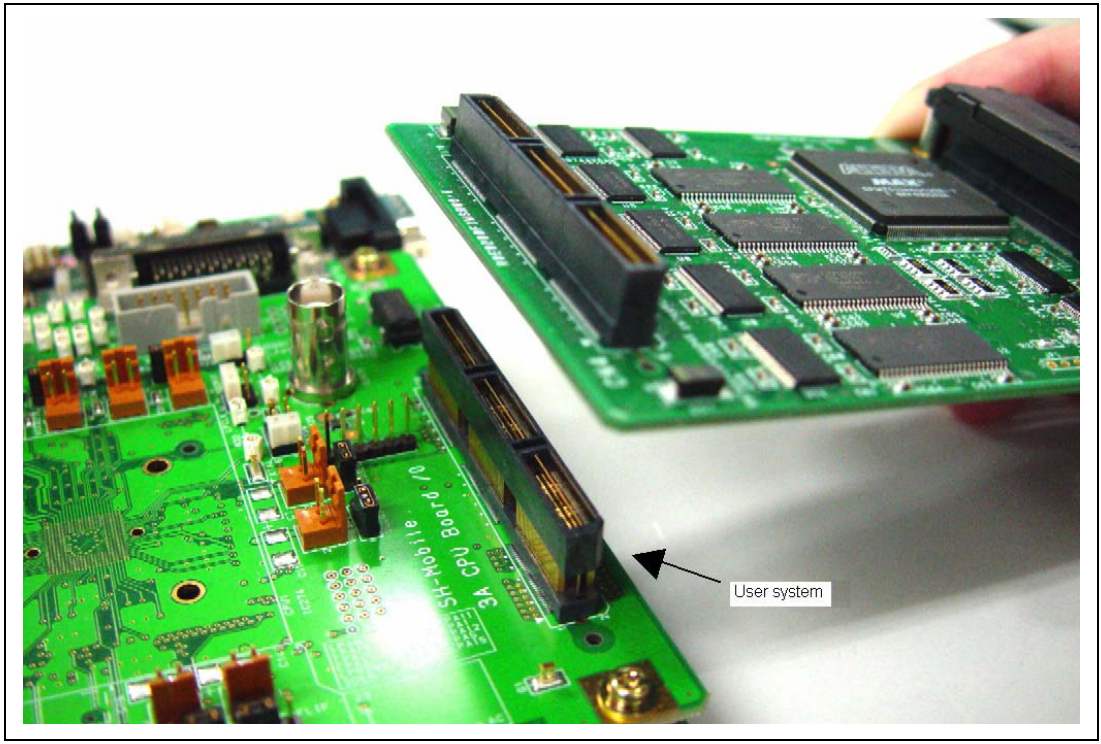


Figure 2.12 Connecting the User System to the Emulation Memory Unit

⚠ CAUTION
Check the location of pin 1 before connecting.

Note: Connection of the signals differs depending on the MCU used.

2.8.5 Connecting the E200F External Bus Trace Unit, Emulation Memory Unit, and User System

- When the external bus trace unit is used with the emulation memory unit, firstly connect the external bus trace unit to the emulation memory unit (figure 2.13) and then to the user system.

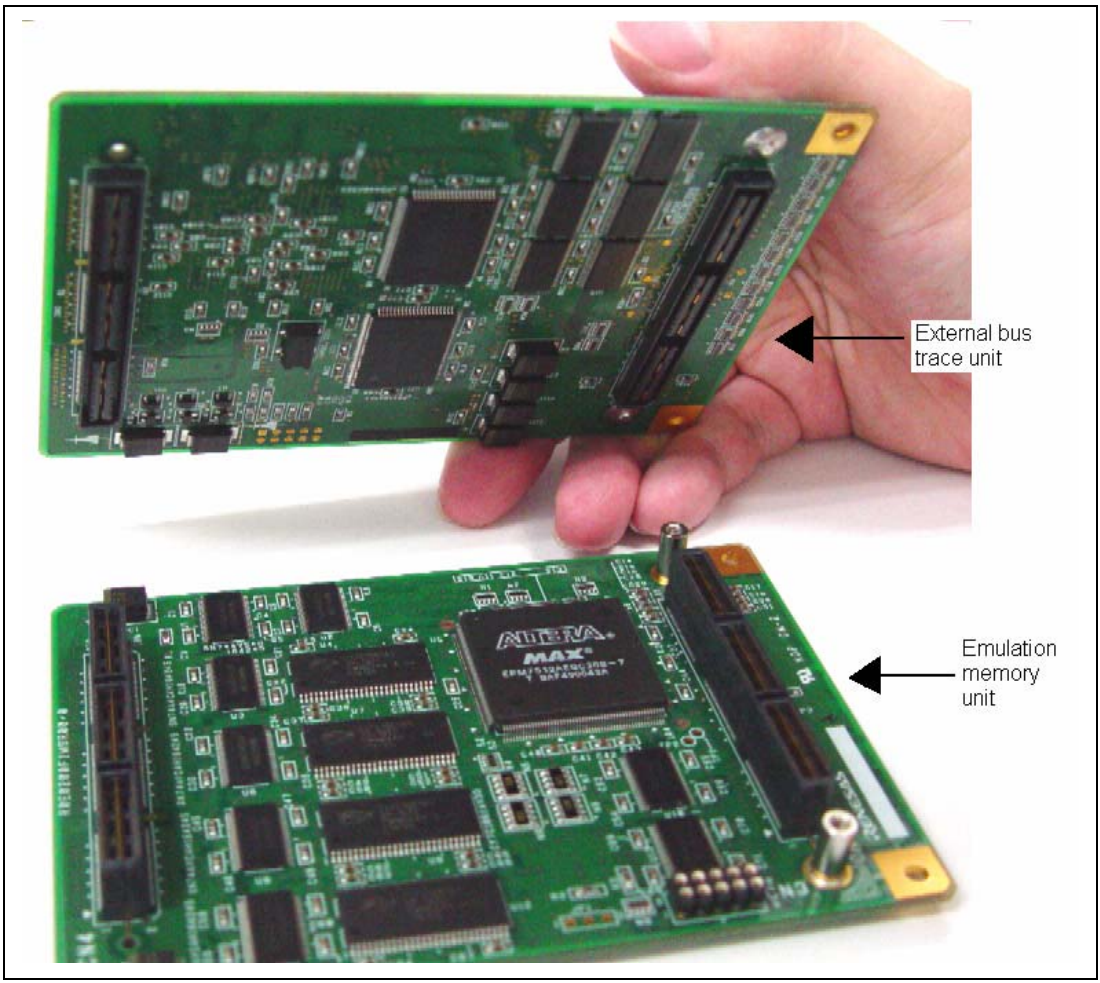


Figure 2.13 Connecting the External Bus Trace Unit to the Emulation Memory Unit

- After checking the location of pin 1, connect the external bus trace unit, emulation memory unit, and trace cable.

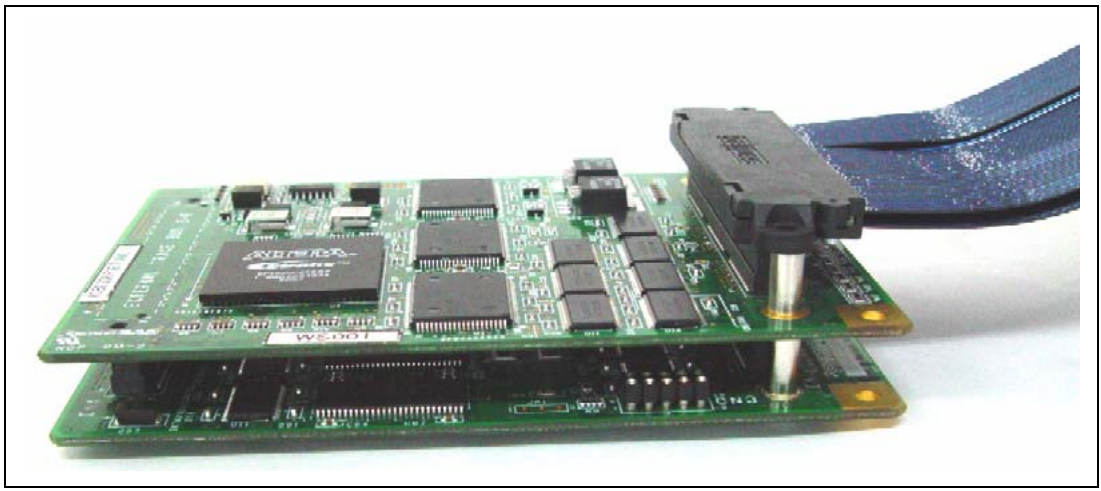


Figure 2.14 Connecting the External Bus Trace Unit, Emulation Memory Unit, and Trace Cable

- After checking the location of pin 1, connect the external bus trace unit, emulation memory unit, and user system.

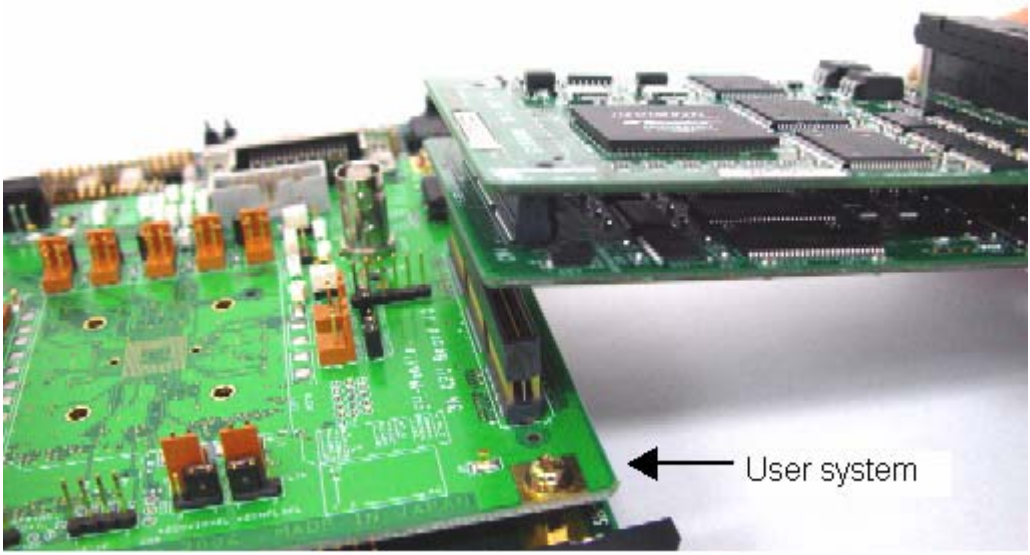


Figure 2.15 Connecting the External Bus Trace Unit, Emulation Memory Unit, and User System

⚠ CAUTION
Check the location of pin 1 before connecting.

Note: Connection of the signals differs depending on the MCU used. For installation and pin assignments of the user system connector, refer to section 2.7, Installing the External Bus Trace Unit Connector.

Section 3 Software Specifications when Using the SH2A_custom_SoC

3.1 Differences between the SH2A_custom_SoC and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 3.1. The initial values of the actual SH2A_custom_SoC registers are undefined. When the emulator is initiated from the workspace, a value to be entered is saved in a session.

Table 3.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	Value of the SP in the power-on reset vector table
PC	Value of the PC in the power-on reset vector table
SR	H'000000F0
GBR	H'00000000
VBR	H'00000000
TBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
FPSCR*	H'00040001
FPUL*	H'00000000
FPR0-15*	H'00000000

Note: If the MCU does not incorporate the floating-point unit (FPU), these registers are not displayed.

Note: When a value of the interrupt mask bit in the SR register is changed in the [Registers] window, it is actually reflected in that register immediately before execution of the user program is started. It also applies when the value is changed by the REGISTER_SET command.

2. The emulator uses the H-UDI; do not access the H-UDI.

3. Low-Power States (Sleep, Software Standby, and Module Standby)
   - When the emulator is used, the sleep state can be cleared with either the clearing function or with the [STOP] button, and a break will occur.
   - The memory must not be accessed or modified in software standby state.
   - The memory must not be accessed or modified in deep standby state.
   - Do not stop inputting the clock to the H-UDI module by using the module standby function.

Note: The memory must not be accessed or modified in software standby state.

4. Reset Signals

   The SH2A_custom_SoC reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the SH2A_custom_SoC.

Note: Do not break the user program when the _RES, _BREQ, or _WAIT signal is being low. A TIMEOUT error will occur. If the _BREQ or _WAIT signal is fixed to low during break, a TIMEOUT error will occur at memory access. The signal names mean the standard signals and may differ according to the MCU in use. In some cases, there will be no corresponding signals.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   During execution of the user program, memory is accessed by the following two methods, as shown in table 3.2; each method offers advantages and disadvantages.

Table 3.2 Memory Access during User Program Execution

Method	Advantage	Disadvantage
H-UDI read/write	The stopping time of the user program is short because memory is accessed by the dedicated bus master.	Cache access is disabled. Actual memory is always accessed by the H-UDI read or write.
Short break	Cache access is enabled.	The stopping time of the user program is long because the user program temporarily breaks.

The method for accessing memory during execution of the user program is specified by using the [Configuration] dialog box.

Table 3.3 Stopping Time by Memory Access (Reference)

Method	Condition	Stopping Time
H-UDI read/write	Reading of one longword for the internal RAM	Reading: Maximum three bus clock cycles (Bϕ)
	Writing of one longword for the internal RAM	Writing: Maximum two bus clock cycles (Bϕ)
Short break	CPU clock: 40 MHz JTAG clock: 1.25 MHz Reading or writing of one byte, one word, or one longword for the external area	About 15 ms

7. Memory Access to the External Flash Memory Area

   The emulator can download the load module to the external flash memory area (for details, refer to section 6.21, Download Function to the Flash Memory Area, in the SH-2A, SH-2 E200F Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or a BREAKPOINT should be set only for the RAM area.

8. Operation while Cache is Enabled

When cache is enabled, the emulator operates as shown in table 3.4.

Table 3.4 Operation while Cache is Enabled

Function	Operation	Notes
Memory write	Searches for whether or not the address to be written hits the instruction and operand caches. • When the address hits, the corresponding position of the data array is changed by the data to be written and single write is performed to the external area. • When the address does not hit, the cache contents are not changed and single write is performed to the external area.	• The contents of the address array are not changed before or after writing of memory.
Memory read	Searches for whether or not the address to be read hits the operand cache. • When the address hits, the corresponding position of the data array is read. • When the address does not hit, single write is performed to the external area.	• The instruction cache is not searched for. • The contents of the address array are not changed before or after reading of memory.
BREAKPOINT	Clears the V and LRU bits of all entries in the instruction cache to 0 if a BREAKPOINT is set or canceled. Clears the V and LRU bits of all entries in the instruction cache to 0 if a break occurs when a BREAKPOINT has been set.	• Use the Event Condition setting if you do not wish to change the contents of the instruction cache.
Program load	Writes the contents of the data cache to the external memory and clears the V and LRU bits of entries in the instruction and data caches to 0 after loading of the program has been completed.	

If memory is read from or written to the disabled cache area, cache is not searched for but the external area is accessed.

9. Multiplexing the AUD Pins in On-Chip Debugging Mode

   The AUD pins are multiplexed with other pins. The AUD function cannot be used for the initial values because they are used as other functions. To use the initial value as the AUD function, set the AUD pins to be used from [AUD pin select] of the [Configuration] dialog box. The emulator rewrites the registers in the pin function controller (PFC) to enable the specified AUD pins before executing the user program. When those registers are changed by the user program, take care so that the settings of the AUD pins is not changed. For details of the setting methods and values, ask Renesas Technology Corp. via the sales office.

10. Using the Watchdog Timer (WDT)

    The WDT does not operate during a break.

11. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be 1.25 MHz.

12. Illegal Instructions

    Do not execute illegal instructions with STEP-type commands.

13. Reset Input

    During execution of the user program, the emulator may not operate correctly if a contention occurs between the following operations for the emulator and the reset input to the target device:

    - Setting an Event Condition
    - Setting an internal trace
    - Displaying the content acquired by an internal trace
    - Reading or writing of a memory

    Note that those operations should not contend with the reset input to the target device.

14. Contention between the Change of the FRQCR Register and the Debugging Functions

    The following notes are required for the user program for changing the multiplication rate of PLL circuit 1 to change the frequency:

    - Avoid contention between the change of the FRQCR register in the user program and the memory access from the [Memory] window, etc.
    - When the automatic updating function is used in the [Monitor] window or [Watch] window, generate and set a break of Event Condition for an instruction immediately before changing the FRQCR register. Contention will be avoided by generating a break and executing the user program again.

    For the change of the multiplication rate of PLL circuit 1 and the FRQCR register, refer to the hardware manual for the MCU.

3.2 Specific Functions for the Emulator when Using the SH2A_custom_SoC

In on-chip debugging mode, a reset must be input when the emulator is activated.

3.2.1 Event Condition Functions

The emulator is used to set event conditions for the following three functions:

- Break of the user program
- Internal trace
- Start or end of performance measurement

Table 3.5 lists the types of Event Condition.

Table 3.5 Types of Event Condition

Event Condition Type	Description
Address bus condition (Address)	Sets a condition when the address bus (data access) value or the program counter value (before or after execution of instructions) is matched.
Data bus condition (Data)	Sets a condition when the data bus value is matched. Byte, word, or longword can be specified as the access data size.
Bus state condition (Bus State)	There are two bus state condition settings: Bus state condition: Sets a condition when the data bus value is matched. Read/write condition: Sets a condition when the read/write condition is matched.
Count	Sets a condition when the other specified conditions are satisfied for the specified counts.
Reset point	A reset point is set when the count and the sequential condition are specified.
Action	Selects the operation when a condition (such as a break, a trace halt condition, a trace acquisition condition, or a trigger output) is matched.

Use the [Combination action (Sequential or PtoP)] dialog box to specify the sequential condition, the point-to-point operation of the internal trace, and the start or end of performance measurement.

Table 3.6 lists the combinations of conditions that can be set under Ch1 to Ch11 and the software trace.

Table 3.6 Dialog Boxes for Setting Event Conditions

		Function				
Dialog Box		**Address Bus Condition (Address)**	**Data Bus Condition (Data)**	**Bus State Condition (Bus Status)**	**Count Condition (Count)**	**Action**
[Event Condition 1]	Ch1	O	O	O	O	O (B, T1, and P)
[Event Condition 2]	Ch2	O	O	O	X	O (B, T1, and P)
[Event Condition 3]	Ch3	O	X	X	X	O (B and T2)
[Event Condition 4]	Ch4	O	X	X	X	O (B and T3)
[Event Condition 5]	Ch5	O	X	X	X	O (B and T3)
[Event Condition 6]	Ch6	O	X	X	X	O (B and T2)
[Event Condition 7]	Ch7	O	X	X	X	O (B and T2)
[Event Condition 8]	Ch8	O	X	X	X	O (B and T2)
[Event Condition 9]	Ch9	O	X	X	X	O (B and T2)
[Event Condition 10]	Ch10	O	X	X	X	O (B and T2)
[Event Condition 11]	Ch11	O (reset point)	X	X	X	O (B and T2)

Notes: 1. O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2. For the Action item,
B: Setting a break is enabled.
T1: Setting the trace halt and acquisition conditions are enabled for the internal trace.
T2: Setting the trace halt is enabled for the internal trace.
T3: Setting the trace halt and point-to-point is enabled for the internal trace.
P: Setting a performance-measurement start or end condition is enabled.

The [Event Condition 11] dialog box is used to specify the count of [Event Condition 1] and becomes a reset point when the sequential condition is specified.

Sequential Setting: Use the [Combination action (Sequential or PtoP)] dialog box to specify the sequential condition and the start or end of performance measurement.

Table 3.7 Conditions to Be Set

Classification	Item	Description
[Ch1, 2, 3] list box	Sets the sequential condition and the start or end of performance measurement using Event Conditions 1 to 3 and 11.	
	Don't care	Sets no sequential condition or the start or end of performance measurement.
	Break: Ch3-2-1	Breaks when a condition is satisfied in the order of Event Condition 3, 2, 1.
	Break: Ch3-2-1, Reset point	Breaks when a condition is satisfied in the order of Event Condition 3, 2, 1. Enables the reset point of Event Condition 11.
	Break: Ch2-1	Breaks when a condition is satisfied in the order of Event Condition 2, 1.
	Break: Ch2-1, Reset point	Breaks when a condition is satisfied in the order of Event Condition 2, 1. Enables the reset point.
	I-Trace stop: Ch3-2-1	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 3, 2, 1.
	I-Trace stop: Ch3-2-1, Reset point	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 3, 2, 1. Enables the reset point.
	I-Trace stop: Ch2-1	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 2, 1.
	I-Trace stop: Ch2-1, Reset point	Halts acquisition of an internal trace when a condition is satisfied in the order of Event Condition 2, 1. Enables the reset point.

Table 3.7 Conditions to Be Set (cont)

Classification	Item	Description
[Ch1, 2, 3] list box (cont)	Ch2 to Ch1 PA	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition).
	Ch1 to Ch2 PA	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition).
[Ch4, 5] list box	Sets the point-to-point of the internal trace (the start or end condition of trace acquisition) using Event Conditions 4 and 5.	
	Don't care	Sets no start or end condition of trace acquisition.
	I-Trace: Ch5 to Ch4 PtoP	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition).
	I-Trace: Ch5 to Ch4 PtoP, Power-on reset	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition) or the power-on reset.

Notes:
1. After the sequential condition and the count specification condition of Event Condition 1 have been set, break and trace acquisition will be halted if the sequential condition is satisfied for the specified count.
2. If a reset point is satisfied, the satisfaction of the condition set in Event Condition will be disabled. For example, if the condition is satisfied in the order of Event Condition 3, 2, reset point, 1, the break or trace acquisition will not be halted. If the condition is satisfied in the order of Event Condition 3, 2, reset point, 3, 2, 1, the break and trace acquisition will be halted.
3. If the start condition is satisfied after the end condition of the performance measurement has been satisfied, performance measurement will be restarted. For the measurement result after a break, the measurement results during performance measurement are added.
4. If the start condition is satisfied after the end condition has been satisfied by the point-to-point of the internal trace, trace acquisition will be restarted.

Usage Example of Sequential Break Extension Setting: A tutorial program provided for the product is used as an example. For the tutorial program, refer to section 6, Tutorial, in the SH-2A, SH-2 E200F Emulator User's Manual.

The conditions of Event Condition are set as follows:

1. Ch1

   Breaks address H'00001086 when the condition [Prefetch address break after executing] is satisfied.
2. Ch2

   Breaks address H'00001068 when the condition [Prefetch address break after executing] is satisfied.
3. Ch3

   Breaks address H'00001058 when the condition [Prefetch address break after executing] is satisfied.

   Note: Do not set other channels.
4. Sets the contents of the [Ch1,2,3] list box to [Break: Ch 3-2-1] in the [Combination action] dialog box.

Then, set the program counter and stack pointer (PC = H'00000800, R15 = H'FFF9F000) in the [Registers] window and click the [Go] button. If this does not execute normally, issue a reset and execute the above procedures.

The program is executed up to the condition of Ch1 and halted. Here, the condition is satisfied in the order of Ch3 -> 2 -> 1.

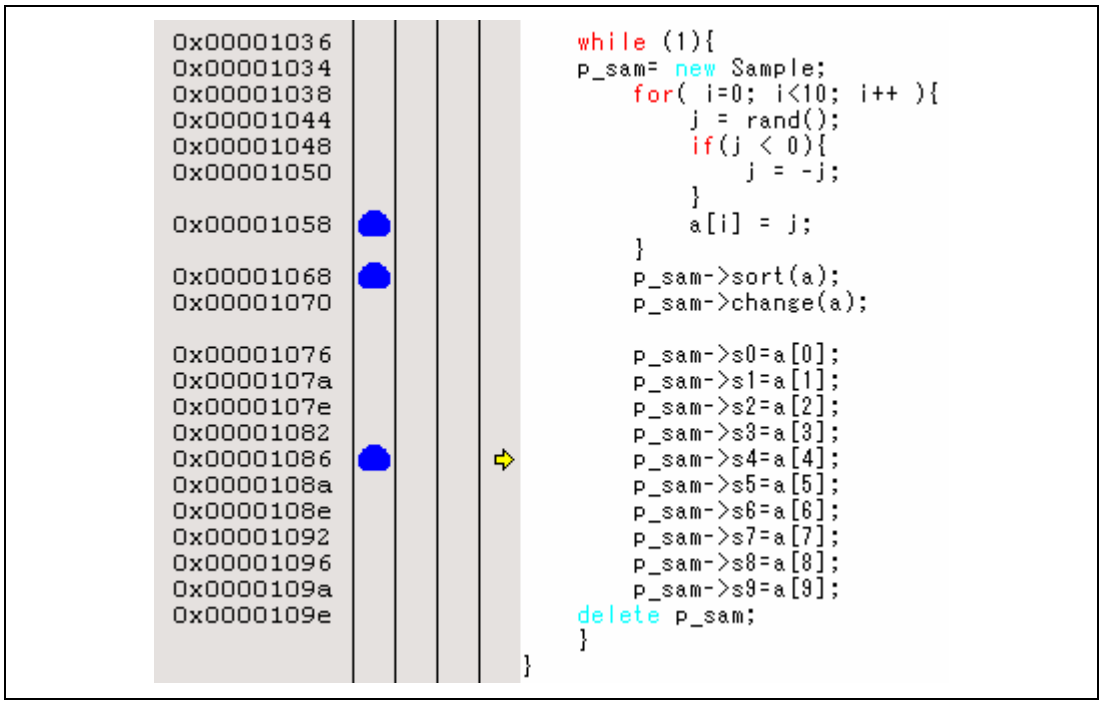


Figure 3.1 [Source] Window at Execution Halt (Sequential Break)

If the sequential condition, performance measurement start/end, or point-to-point for the internal trace is set, conditions of Event Condition to be used will be disabled. Such conditions must be enabled from the popup menu by clicking the right mouse button on the [Event Condition] sheet.

Notes:
1. If the Event condition is set for the slot in the delayed branch instruction by the program counter (after execution of the instruction), the condition is satisfied before executing the instruction in the branch destination (when a break has been set, it occurs before executing the instruction in the branch destination).
2. Do not set the Event condition for the SLEEP instruction by the program counter (after execution of the instruction).
3. When the Event condition is set for the 32-bit instruction by the program counter, set that condition in the upper 16 bits of the instruction.
4. If the power-on reset and the Event condition are matched simultaneously, no condition will be satisfied.
5. Do not set the Event condition for the DIVU or DIVS instruction by the program counter (after execution of the instruction).

6. If a condition of which intervals are satisfied closely is set, no sequential condition will be satisfied.
   - Set the Event conditions, which are satisfied closely, by the program counter with intervals of two or more instructions.
   - After the Event condition has been matched by accessing data, set the event condition by the program counter with intervals of 17 or more instructions.
7. If the settings of the Event condition or the sequential conditions are changed during execution of the program, execution will be suspended. (The number of clock cycles to be suspended during execution of the program is a maximum of about 102 bus clock cycles (Bϕ). If the bus clock (Bϕ) is 66.6 MHz, the program will be suspended for 1.53 μs.)
8. If the settings of Event conditions or the sequential conditions are changed during execution of the program, the emulator temporarily disables all Event conditions to change the settings. During this period, no Event conditions will be satisfied.
9. If the break condition before executing an instruction is set to the instruction followed by DIVU and DIVS, the factor for halting a break will be incorrect under the following condition:
   If a break occurs during execution of the above DIVU and DIVS instructions, the break condition before executing an instruction, which has been set to the next instruction, may be displayed as the factor for halting a break.
10. If the break conditions before and after executing instructions are set to the same address, the factor for halting a break will be incorrectly displayed. The factor for halting a break due to the break condition after executing an instruction will be displayed even if a break is halted by the break condition before executing an instruction.
11. Do not set the break condition after executing instructions and BREAKPOINT (software break) to the same address.
12. When the emulator is being connected, the user break controller (UBC) function is not available.

3.2.2 Trace Functions

The emulator supports the trace functions listed in table 3.8.

Table 3.8 Trace Functions

Function	Internal Trace	AUD Trace
Branch trace	Supported	Supported
Memory access trace	Supported	Supported
Software trace	Not supported	Supported

The internal and AUD traces are set in the [I-Trace/AUD-Trace acquisition] dialog box of the [Trace] window.

Internal Trace Function: When [I-Trace] is selected for [Trace type] on the [Trace mode] page of the [I-Trace/AUD-Trace acquisition] dialog box, the internal trace can be used.

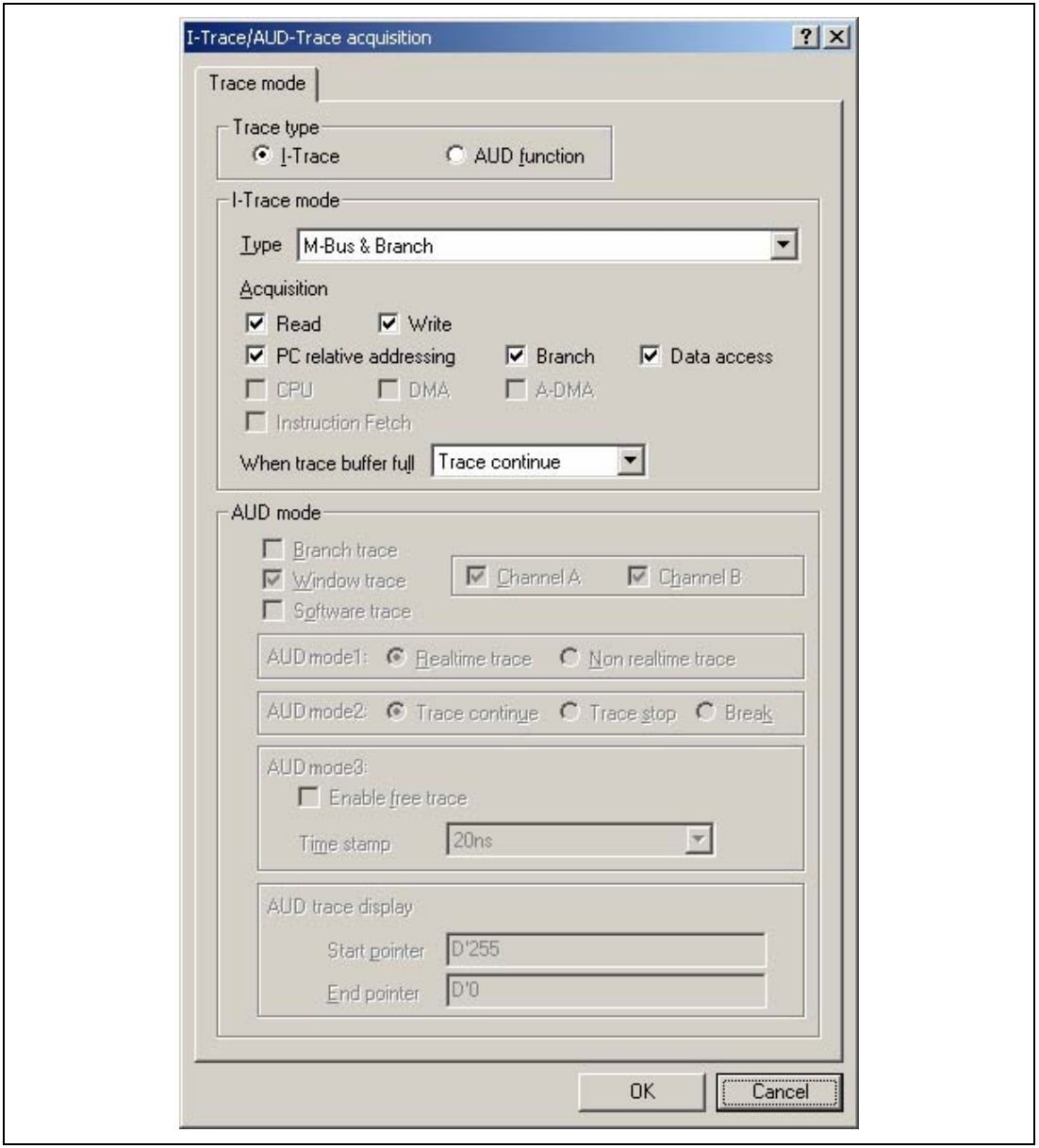


Figure 3.2 [I-Trace/AUD-Trace acquisition] Dialog Box (Internal Trace Function)

The following three items can be selected as the internal trace from [Type] of [I-Trace mode].

Table 3.9 Information on Acquiring the Internal Trace

Item	Acquisition Information
[M-Bus & Branch]	Acquires the data and branch information on the M-bus. • Data access (read/write) • PC-relative access • Branch information
[I-Bus]	Acquires the data on the I-bus. • Data access (read/write) • Selection of the bus master on the I-bus (CPU/DMA/A-DMA) • Instruction fetch
[I-Bus, M-Bus & Branch]	Acquires the contents of [M-Bus & Branch] and [I-Bus].

After selecting [Type] of [I-Trace mode], select the contents to be acquired from [Acquisition]. Typical examples are described below (note that items disabled for [Acquisition] are not acquired).

- Example of acquiring branch information only:
  Select [M-Bus & Branch] from [Type] and enable [Branch] on [Acquisition].
- Example of acquiring the read or write access (M-bus) only by the user program:
  Select [M-Bus & Branch] from [Type] and enable [Read], [Write], and [Data access] on [Acquisition].
- Example of acquiring the read access only by DMAC (I-bus):
  Select [I-Bus] from [Type] and enable [Read], [DMA], and [Data access] on [Acquisition].

Using the Event Condition restricts the condition; the following three items are set as the internal trace conditions.

Table 3.10 Trace Conditions of the Internal Trace

Item	Acquisition Information
Trace halt	Acquires the internal trace until the Event Condition is satisfied. (The trace content is displayed in the [Trace] window after a trace has been halted. No break occurs in the user program.)
Trace acquisition	Acquires only the data access where the Event Condition is satisfied.
Point-to-point	Traces the period from the satisfaction of Event Condition 5 to the satisfaction of Event Condition 4.

To restrict trace acquisition to access only a specific address or specific function of a program, an Event Condition can be used. Typical examples are described below.

- Example of halting a trace with a write access (M-bus) to H'FFF80000 by the user program as a condition (trace halt):

  Set the condition to be acquired on [I-Trace mode].

  Set the following in the [Event Condition 1] or [Event Condition 2] dialog box:

  Address condition: Set [Address] and H'FFF80000.

  Bus state condition: Set [M-Bus] and [Write].

  Action condition: Disable [Acquire Break] and set [Acquire Trace] for [Stop].

- Example of acquiring the write access (M-bus) only to H'FFF80000 by the user program (trace acquisition condition):

  Select [M-Bus & Branch] from [Type] and enable [Write] and [Data access] on [Acquisition].

  Set the following in the [Event Condition 1] or [Event Condition 2] dialog box:

  Address condition: Set [Address] and H'FFF80000.

  Bus state condition: Set [M-Bus] and [Write].

  Action condition: Disable [Acquire Break] and set [Acquire Trace] for [Condition].

For the trace acquisition condition, the condition to be acquired by the Event Condition should be acquired by setting the [I-Trace mode].

- Example of acquiring a trace for the period while the program passes H'1000 through H'2000 (point-to-point):

  Set the condition to be acquired on [I-Trace mode].

  Set the address condition as H'1000 in the [Event Condition 4] dialog box.

Set the address condition as H'2000 in the [Event Condition 5] dialog box.

Set [I-Trace] as [Ch4 to Ch5 PtoP] in the [Combination action (Sequential or PtoP)] dialog box.

When point-to-point and trace acquisition condition are set simultaneously, they are ANDed.

Notes on Internal Trace:

- Timestamp

  The timestamp is the clock counts of Bϕ (48-bit counter). Table 3.11 shows the timing for acquiring the timestamp.

Table 3.11 Timing for the Timestamp Acquisition

Item	Acquisition Information	Counter Value Stored in the Trace Memory
M-bus data access		Counter value when data access (read or write) has been completed
Branch		Counter value when the next bus cycle has been completed after a branch
I-bus	Fetch	Counter value when a fetch has been completed
	Data access	Counter value when data access has been completed

- Point-to-point

  The trace-start condition is satisfied when the specified instruction has been fetched. Accordingly, if the trace-start condition has been set for the overrun-fetched instruction (an instruction that is not executed although it has been fetched at a branch or transition to an interrupt), tracing is started during overrun-fetching of the instruction. However, when overrun-fetching is achieved (a branch is completed), tracing is automatically suspended.
  If the start and end conditions are satisfied closely, trace information will not be acquired correctly.
  The execution cycle of the instruction fetched before the start condition is satisfied may be traced.
  When the I-bus is acquired, do not specify point-to-point.
  Memory access may not be acquired by the internal trace if it occurs at several instructions immediately before satisfaction of the point-to-point end condition.

- Halting a trace

  Do not set the trace-end condition for the SLEEP instruction and the branch instruction that the delay slot becomes the SLEEP instruction.

- Trace acquisition condition

  Do not set the trace-end condition for the SLEEP instruction and the branch instruction according to which the delay slot becomes the SLEEP instruction.
  When [I-BUS, M-Bus & Branch] is selected and the trace acquisition condition is set for the M-bus and I-bus with the Event Condition, set the M-bus condition and the I-bus condition for [Event Condition 1] and [Event Condition 2], respectively.
  If the settings of [I-Trace mode] are changed during execution of the program, execution will be suspended. (The number of clock cycles to be suspended during execution of the program is a maximum of about 51 peripheral clock cycles (Pϕ) + 15 bus clock cycles (Bϕ). If the peripheral clock (Pϕ) is 33.3 MHz and the bus clock (Bϕ) is 66.6 MHz, the program will be suspended for 1.757 μs.)

- Displaying a trace

  If a trace is displayed during execution of the program, execution will be suspended to acquire the trace information. (The number of clock cycles to be suspended during execution of the program is a maximum of about 20480 peripheral clock cycles (Pϕ) + 4096 bus clock cycles (Bϕ). If the peripheral clock (Pϕ) is 33.3 MHz and the bus clock (Bϕ) is 66.6 MHz, the program will be suspended for 676.52 μs.)

- Branch trace

  If breaks occur immediately after executing non-delayed branch and TRAPA instructions and generating a branch due to exception or interrupt, a trace for one branch will not be acquired immediately before such breaks.
  However, this does not affect on generation of breaks caused by a BREAKPOINT and a break before executing instructions of Event Condition.

AUD Trace Functions: This function is operational when the AUD pins of the MCU are connected to the emulator. Table 3.12 shows the AUD trace acquisition mode that can be set in each trace function.

Table 3.12 AUD Trace Acquisition Mode

Type	Mode	Description
Continuous trace occurs	Realtime trace	When the next branching occurs while the trace information is being output, all the information may not be output. The user program can be executed in realtime, but some trace information will be lost.
	Non realtime trace	When the next branching occurs while the trace information is being output, the CPU stops operations until the information is output. The user program is not executed in realtime.
Trace buffer full	Trace continue	This function writes the latest trace information on the oldest information to store the latest trace information.
	Trace stop	After the trace buffer becomes full, the trace information is no longer acquired. The user program is continuously executed.
	Break	A break occurs when the trace buffer becomes full.
AUD trace function used	Enable free trace	When this box is checked, the emulator ignores the AUD eventpoint setting and acquires all trace information.
	Time stamp clock	The resolution of the timer for timestamps can be specified. Select 20 ns, 100 ns, 400 ns, or 1.6 μs.

To set the AUD trace acquisition mode, click the [Trace] window with the right mouse button and select [Setting] from the pop-up menu to display the [I-Trace/AUD-Trace acquisition] dialog box. The AUD trace acquisition mode can be set in the [AUD mode1], [AUD mode2], or [AUD mode3] group box in the [Trace mode] page of the [I-Trace/AUD-Trace acquisition] dialog box.

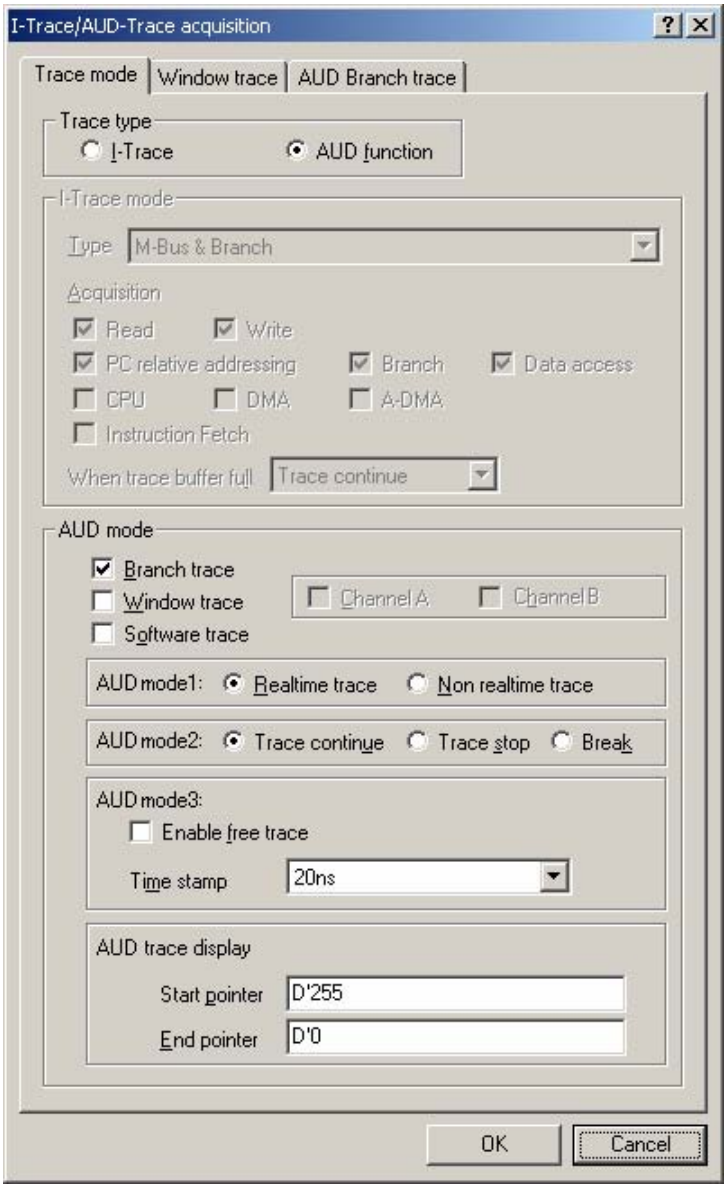


Figure 3.3 [Trace mode] Page

When the AUD trace function is used, select the [AUD function] radio button in the [Trace type] group box of the [Trace mode] page.

(a) Branch Trace Function

The branch source and destination addresses and their source lines are displayed.

Branch trace can be acquired by selecting the [Branch trace] check box in the [AUD function] group box of the [Trace mode] page.

The branch type can be selected in the [AUD Branch trace] page.

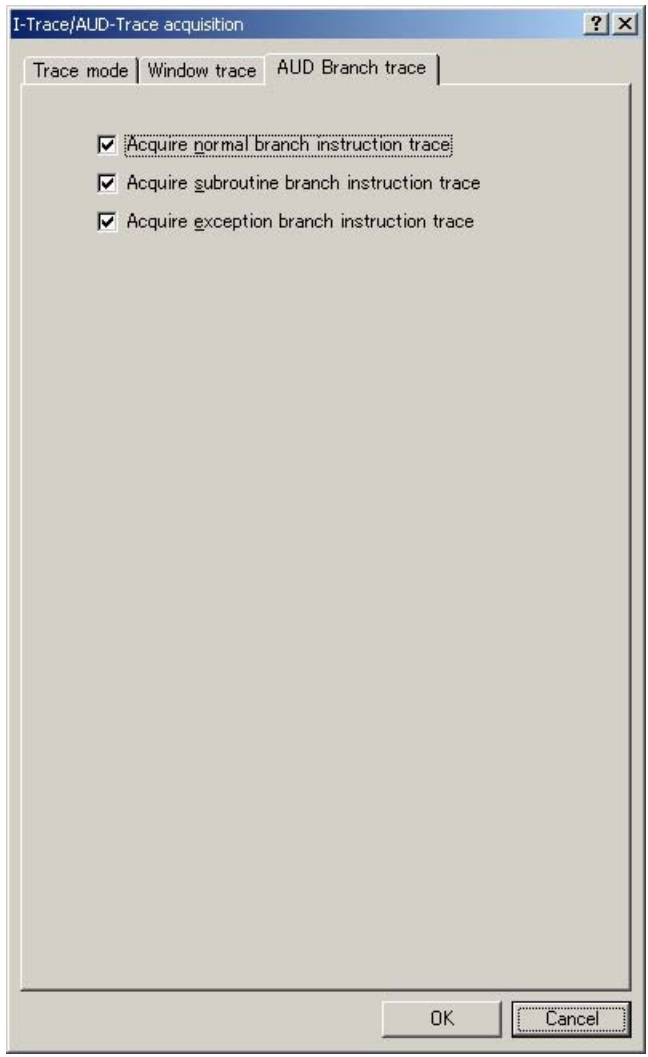


Figure 3.4 [AUD Branch trace] Page

(b) Window Trace Function

Memory access in the specified range can be acquired by trace.

Two memory ranges can be specified for channels A and B. The read, write, or read/write cycle can be selected as the bus cycle for trace acquisition.

Setting Method:

(i) Select the [Channel A] and [Channel B] check boxes in the [AUD function] group box of the [Trace mode] page. Each channel will become valid.

(ii) Open the [Window trace] page and specify the bus cycle and memory range that are to be set for each channel.

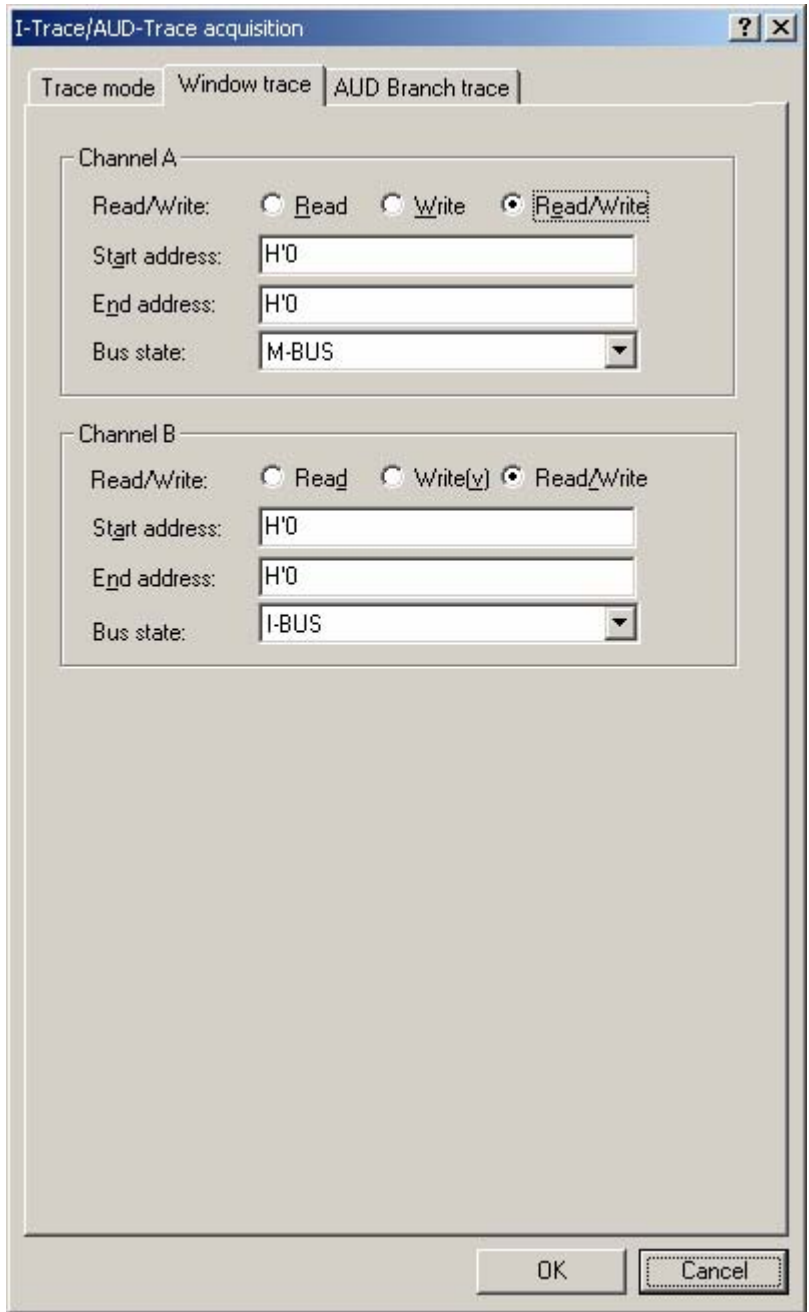


Figure 3.5 [Window trace] Page

Note: When [M-BUS] or [I-BUS] is selected, the following bus cycles will be traced.

- M-BUS: A bus cycle generated by the CPU is acquired. A bus cycle is also acquired when the cache has been hit.
- I-BUS: A bus cycle generated by the CPU or DMA is acquired. A bus cycle is not acquired when the cache has been hit.

(c) Software Trace Function

Note: This function can be supported with SuperH C/C++ compiler (manufactured by Renesas Technology Corp.; including OEM and bundle products) V7.0 or later.

When a specific instruction is executed, the PC value at execution and the contents of one general register are acquired by trace. Describe the Trace(x) function (x is a variable name) to be compiled and linked beforehand. For details, refer to the SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual.

When the load module is downloaded on the emulator and is executed while a software trace function is valid, the PC value that has executed the Trace(x) function, the general register value for x, and the source lines are displayed.

To activate the software trace function, select the [Software trace] check box in the [AUD function] group box of the [Trace mode] page.

Notes on AUD Trace:

1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.
2. The AUD trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previous branch source address is the same for the upper 16 bits, the lower 16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
   The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.
3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. In the emulator, when multiple loops are performed to reduce the number of AUD trace displays, only the IP counts up.
5. In the emulator, the maximum number of trace displays is 262144 lines (131072 branches). However, the maximum number of trace displays differs according to the AUD trace information to be output. Therefore, the above pointers cannot always be acquired.

6. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
7. The AUD trace is disabled while the profiling function is used.
8. If breaks occur immediately after executing non-delayed branch and TRAPA instructions and generating a branch due to exception or interrupt, a trace for one branch will not be acquired immediately before such breaks.
   However, this does not affect on generation of breaks caused by a BREAKPOINT and a break before executing instructions of Event Condition.
9. For the result by software trace, a value in the [Data] item is not correct (that value is correct for window trace).

3.2.3 Notes on Using the JTAG (H-UDI) Clock (TCK) and AUD Clock (AUDCK)

1. Set the JTAG clock (TCK) frequency to lower than the frequency of the peripheral module clock.
2. The initial value of the JTAG clock (TCK) is 1.25 MHz.
3. A value to be set for the JTAG clock (TCK) is initialized after executing [Reset CPU] or [Reset Go]. Thus the TCK value will be 1.25 MHz.
4. Set the AUD clock (AUDCK) frequency to 50 MHz or lower. If the frequency is higher than 50 MHz, the emulator will not operate normally.

3.2.4 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address.
   It cannot be set to the following addresses:
   - An area other than CS and the internal RAM
   - An instruction in which Event Condition 2 is satisfied
   - A slot instruction of a delayed branch instruction
3. During step operation, the specified BREAKPOINT and Event Condition breaks are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified and a break occurs before the Event Condition execution, single-step operation is performed at the address before execution resumes. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.

6. If a BREAKPOINT cannot be correctly set to an address in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the break condition, the mark ● disappears.
7. If you wish to use a BREAKPOINT (software break), specify the SH2A_SBSTK command to enable use of a user stack before setting a PC break. While enabled, extra four bytes of a user stack are used when a break occurs. The value of the stack pointer (R15) must be correctly set in advance because a user stack is to be used. By default, use of a user stack is disabled. For details on the command, refer to the help file.

- Example
  To enable use of a user stack:
  >SH2A_SBSTK enable

3.2.5 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.

3.2.6 Performance Measurement Function

The emulator supports the performance measurement function.

1. Setting the performance measurement conditions
   To set the performance measurement conditions, use the [Performance Analysis] dialog box or the PERFORMANCE_SET command. When any line in the [Performance Analysis] window is clicked with the right mouse button, a popup menu is displayed and the [Performance Analysis] dialog box can be displayed by selecting [Setting].

Note: For the command line syntax, refer to the online help.

(a) Specifying the measurement start/end conditions
   The measurement start/end conditions are specified by using Event Condition 1,2. The [Ch1,2,3] list box of the [Combination action] dialog box can be used.

Table 3.13 Measurement Period

Classification	Item	Description
Selection in the [Ch1, 2, 3] list box	Ch2 to Ch1 PA	The period from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition) is set as the performance measurement period.
	Ch1 to Ch2 PA	The period from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition) is set as the performance measurement period.
	Other than above	The period from the start of execution of the user program to the occurrence of a break is measured.

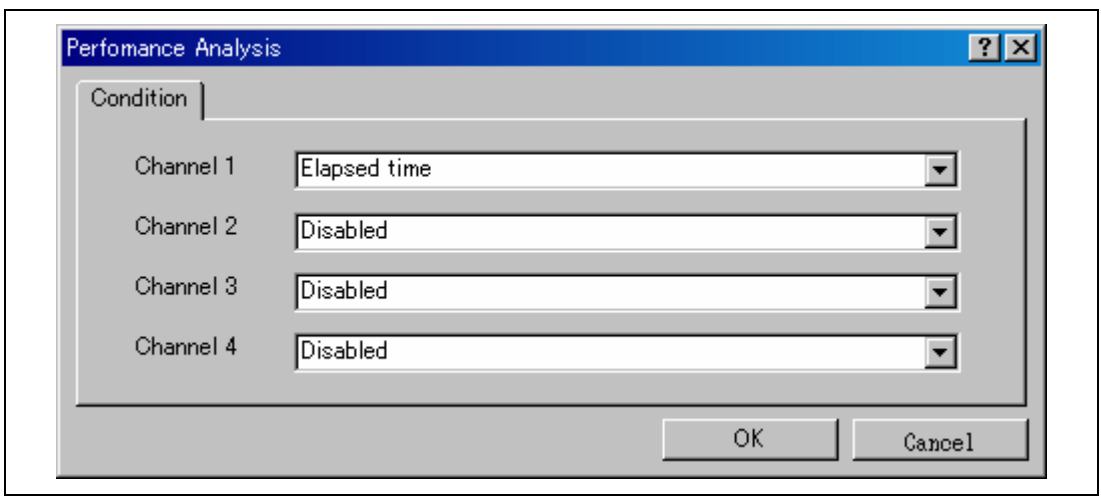


Figure 3.6 [Performance Analysis] Dialog Box

For measurement tolerance,

- The measured value includes tolerance.
- Tolerance will be generated before or after a break.

Note: When [Ch2 to Ch1 PA] or [Ch1 to Ch2 PA] is selected, to execute the user program, specify conditions set in Event Condition 2 and Event Condition 1 and one or more items for performance measurement.

(b) Measurement item

Items are measured with [Channel 1 to 4] in the [Performance Analysis] dialog box. Maximum four conditions can be specified at the same time. Table 3.14 shows the measurement items (Options in table 3.14 are parameters for <mode> of the PERFORMANCE_SET command. They are displayed for CONDITION in the [Performance Analysis] window).

Table 3.14 Measurement Item

Selected Name	Option
Disabled	None
Elapsed time	AC
Branch instruction counts	BT
Number of execution instructions	I
Number of execution 32bit-instructions	I32
Exception/interrupt counts	EA
Interrupt counts	INT
Data cache-miss counts	DC
Instruction cache-miss counts	IC
All area access counts	ARN
All area instruction access counts	ARIN
All area data access counts	ARND
Cacheable area access counts	CDN (data access)
Cacheable area instruction access counts	CIN
Non cacheable area data access counts	NCN
URAM area access counts	UN
URAM area instruction access counts	UIN
URAM area data access counts	UDN
Internal I/O area data access counts	IODN
Internal ROM area access counts	RN
Internal ROM area instruction access counts	RIN
Internal ROM area data access counts	RDN
All area access cycle	ARC
All area instruction access cycle	ARIC
All area data access cycle	ARDC
All area access stall	ARS
All area instruction access stall	ARIS
All area data access stall	ARDS

Note: Selected names are displayed for CONDITION in the [Performance Analysis] window.
Options are parameters for <mode> of the PERFORMANCE_SET command.

Notes: 1. In the non-realtime trace mode of the AUD trace, normal counting cannot be performed because the generation state of the stall or the execution cycle is changed.
2. If the internal ROM is not installed on the product, do not set the measurement item for the internal ROM area.

2. Displaying the measured result

The measured result is displayed in the [Performance Analysis] window or the PERFORMANCE_ANALYSIS command in hexadecimal (32 bits).

Note: If a performance counter overflows as a result of measurement, "********" will be displayed.

3. Initializing the measured result

To initialize the measured result, select [Initialize] from the popup menu in the [Performance Analysis] window or specify INIT with the PERFORMANCE_ANALYSIS command.

SH-2A, SH-2 E200F Emulator
Additional Document for User's Manual
Supplementary Information on Using the SH2A_custom_SoC

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SH-2A, SH-2 E200F Emulator Additional Document for User's Manual Supplementary Information on Using the SH2A_custom_SoC

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